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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,267	01/02/2004	Peter J. Zdebel	ONS00535	1730

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,267	ZDEBEL ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *32-38* is/are withdrawn from consideration.

5)☒ Claim(s) *20-31* is/are allowed.

6)☒ Claim(s) *1,5-10 and 15-17* is/are rejected.

7)☒ Claim(s) *2-4,11-14,18 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-2-04 & 5-23-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed January 2, 2004.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-31, drawn to a semiconductor ESD structured, classified in class 257, subclass 356.

II. Claims 32-38, drawn to a method for forming a semiconductor device, classified in class 438, subclass 197.

The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). Unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, since the device of the Group I invention could be made by a process materially different from those/that of the Group II invention. In the instant case, the process as claimed can be used to make other and materially different product.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Kevin B. Jackson on August 3, 2005 a provisional election was made without traverse to prosecute the invention of a semiconductor ESD structure, claims 1-31. Affirmation of this election must be made by applicant in replying to this Office action. Claims 32-38 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-10 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (5,545,909) in view of Williams (6,060,752).

In regard to claim 1, Williams et al. teach a semiconductor ESD structure comprising: a semiconductor substrate 1442 of a first conductivity type having a first region 1444 of a second conductivity type and a first dopant concentration; a buried region 1416 of the second conductivity type formed in the first region 1444; a second region 1400 of the first conductivity type formed in the first region 1444; a third region 1408 of the first conductivity type formed in the first region 1444; a first isolation region 1418-center formed in the first region 1444 between the second 1400 and third 1408 regions; a first pair 1402 of oppositely doped regions formed in the second region 1400; and a second pair 1410 of oppositely doped regions formed in the third region 1408 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

However, Williams et al. fail to teach the second and third regions contacting the buried layer.

Williams teaches second 904 and third 910 regions contacting buried layers 926 & 928 (Figure 9A, columns 6-7, lines 53-67 and 1-18, respectively).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor ESD structure as taught by Williams et al. with the semiconductor ESD structure having second and third regions contacting the buried layers as taught by Williams to protect against damage resulting from excessively high or low voltage swings such as those created by electrostatic

discharges, particularly voltage swings which rise to a level that is above the supply voltage providing power to the circuit (column 1, lines 6-10).

In regard to claim 5, Williams et al. teach the first isolation region 1418-center extending through the first region 1444 and contacting the buried region 1416 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 6, Williams et al. teach the first region 1444 comprising an epitaxial layer (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 7, Williams et al. teach the first pair 1402 of oppositely doped regions being shorted together (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 8, Williams et al. teach the second pair 1410 of oppositely doped regions being shorted together (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 9, Williams et al. teach a second isolation region 1418-left formed in the first region 1444 adjacent the second region 1400; and a third isolation region 1418-right formed in the first region 1444 adjacent the third region 1408 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 10, Williams et al. teach the second 1418-third and third 1418-right regions extending to the buried layer 1416 (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively).

In regard to claim 15, Williams et al. teach the buried region 1416 and the second region 1400 form a buried avalanche region (Figure 14, column 12, lines 13-25).

In regard to claim 16, Williams et al. teach the buried region 1416 and the third region 1408 form a buried avalanche region (Figure 14, column 12, lines 13-25).

In regard to claim 17, Williams et al. teach one of the first pair 1402 of oppositely doped regions and the second pair 1410 of oppositely doped regions being shorted together (Figure 14, columns 8-10, lines 58-67, 1-67 and 1-10, respectively). And in regard to the fact one of the first pair and second pair are shorted together, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function, In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959). Apparatus claims cover what a device is, not what a device does. Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Allowable Subject Matter

Claims 20-31 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as a first ring region of a first conductivity type formed in a layer semiconductor material of a second conductivity type and having a first doping concentration; a second ring region of the first conductivity type formed in the layer of semiconductor material; a first doped region of the second conductivity type within the layer of semiconductor material and coupled to the first and second ring regions; and a

third ring region comprising an isolation region between the first and second ring regions. The dependent claims being further limiting and definite are also allowable.

Claims 2-4, 11-14 and 18-19 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor ESD structures:

Bulucea et al. (5,952,701) Kaizu et al. (5,517,224)

Kato et al. (US 2003/0230777 A1) Matsunaga et al. (5,238,850)

Sato et al. (US 2002/0109191 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
August 7, 2005

John M. Guerrero
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